SEP 03 2008
PATENT & TRADEMARK OFFICE

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Docket No.: SON-1582
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Masumitsu INO et al.

Application No.: 09/424,544 Confirmation No.: 8128

Filed: November 24, 1999 Art Unit: 2629

For: LIQUID CRYSTAL DISPLAY Examiner: J. J. Piziali

RESPONSE TO NOTICE OF NON-COMPLIANT APPEAL BRIEF (37 C.F.R. 41.37) AND TRANSMITTAL OF APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is in response to the Notice of Non-Compliant Appeal Brief (37 C.F.R. 41.37) mailed on August 27, 2008.

An Appellant's Brief on Appeal for the above-referenced application is being filed herewith. An Appeal Brief and fee was filed on August 15, 2008.

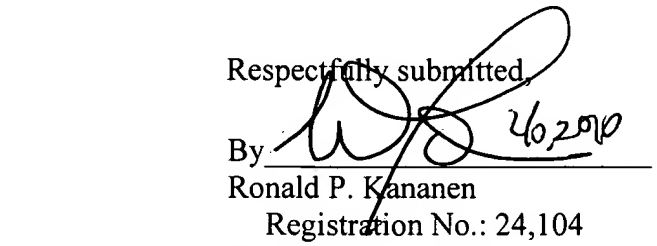
Pursuant to practice and procedures within the U.S. Patent and Trademark Office, any previously paid appeal fees set forth in 37 CFR 41.20 for filing a notice of appeal, filing an appeal brief, and requesting an oral hearing (if applicable) will be applied to the new appeal on the same application as long as a final Board decision has not been made on the prior appeal. M.P.E.P. §1204.01.

Please apply the fee paid on August 15, 2008 for the Appeal Brief Transmittal.

If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

Dated: September 3, 2008

Respectfully submitted,



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APPELLANT'S BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

This is an Appeal Brief under 37 C.F.R. §41.37 appealing the final decision of the Examiner dated May 28, 2008. Each of the topics required by 37 C.F.R. §41.37 is presented herewith and is labeled appropriately.

This brief is in furtherance of the Final Office Action of May 28, 2008.

In response to a previous Final Office Action mailed on November 3, 2003, a Notice of Appeal was filed in this case on February 4, 2004.

An Appeal Brief Transmittal was filed in this case on April 2, 2004.

A non-final Office Action mailed on November 30, 2006 ***withdrew*** the previous Final Office Action of November 3, 2003 and ***reopened prosecution*** in this case.

A new Final Office Action has been mailed in this case on May 28, 2008.

Pursuant to practice and procedures within the U.S. Patent and Trademark Office, any previously paid appeal fees set forth in 37 CFR 41.20 for filing a notice of appeal, filing an appeal brief, and requesting an oral hearing (if applicable) will be applied to the new appeal on the same application as long as a final Board decision has not been made on the prior appeal. M.P.E.P. §1204.01.

Here, a new Notice of Appeal and a new Appeal Brief Transmittal that apply the previously paid appeal fees have been filed along with the present Appellant's Brief.

Accordingly, the filing of this Appellant's Brief is timely. 37 C.F.R. §1.136.

I. REAL PARTY IN INTEREST

Sony Corporation of Tokyo, Japan ("Sony") is the real party in interest of the present application. An assignment of all rights in the present application to Sony was executed by the inventor and recorded by the U.S. Patent and Trademark Office at **reel 010555, frame 0866.**

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Within the Final Office Action of May 28, 2008, the status of the claims is as follows:

Claims 1-24 (canceled);

Claims 25-29 (rejected);

Claim 30 (canceled);

Claim 31 (rejected);

Claims 32-36 (canceled);

Claim 37 (rejected);

Claims 38-42 (canceled);

Claims 43-78 (rejected).

No claims are indicated within the Final Office Action to contain allowable subject matter.

Accordingly, Appellant hereby appeals the final rejection of claims 25-29, 31, 37, and 43-78, which are presented in the Claims Appendix.

IV. STATUS OF AMENDMENTS

Subsequent to the final rejection of May 28, 2008, ***no amendment*** has been filed on February 4, 2004.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to a liquid crystal display (LCD) and, more particularly, to a matrix type liquid crystal display in which a driver circuit to apply a signal potential to each pixel is provided as an external circuit of a liquid crystal display panel.

Claim 25 - Claim 25 includes the features of:

a display portion 10 (specification at figure 5), said display portion 10 having a plurality of gate lines 11, a plurality of signal lines 12 and a plurality of pixels 20 (specification at figure 3, page 9, lines 5-17),

a pixel 20 of said plurality of pixels 20 being located at an intersection of a gate line 11 of said plurality of gate lines 11 and a signal line 12 of said plurality of signal lines 12 (specification at figure 3); and

a plurality of driver circuits 14, 44 (specification at page 19, lines 5-6), said plurality of driver circuits 14, 44 including at least one general driver circuit and one remainder driver circuit (specification at figure 5),

each said at least one general driver circuit 14, 44 having a general driver horizontal shift register circuit 31 (specification at figure 4, page 11, line 26 to page 12, line 1) and a plurality of general driver circuit output terminals, a general driver circuit output terminal of said plurality of general driver circuit output terminals providing a signal potential to one of said plurality of signal lines (specification at page 19, lines 5-6),

said remainder driver circuit having a remainder driver horizontal shift register circuit 31 (specification at figure 4, page 11, line 26 to page 12, line 1) and a plurality of remainder driver circuit output terminals, a remainder driver circuit output terminal of said plurality of remainder driver circuit output terminals providing another signal potential to another of said plurality of signal lines (specification at figure 5),

the quantity of remainder driver circuit output terminals being defined as (S – (OP * (DC-1))) (specification at figure 5, page 13, lines 18-21), "S" being the quantity of said plurality of signal lines 12 (specification at page 13, lines 10-13), "OP" being the quantity of general driver circuit output terminals, and "DC" being the quantity of said plurality of driver circuits 14 (specification at figure 5, page 13, lines 21-26),

said quantity of general driver circuit output terminals being different than said quantity of remainder driver circuit output terminals (specification at figure 5).

Claim 48 - Claim 48 is dependent upon claim 25. Within claim 48, the plurality of driver circuits are driver integrated circuits arranged in an outside of a transparent insulating substrate on which said display portion is formed (specification at figure 5).

Claim 49 - Claim 49 is drawn to a liquid crystal display comprising:

a display portion 10 (specification at Figure 6), said display portion 10 having a plurality of gate lines 11, a plurality of signal lines 12 and a plurality of pixels 20 (specification at figure 3, page 9, lines 5-17),

a pixel 20 of said plurality of pixels 20 being located at an intersection of a gate line 11 of said plurality of gate lines 11 and a signal line 12 of said plurality of signal lines 12 (specification at figure 3), and

a plurality of driver circuits 14, 44, each of said plurality of driver circuits 14, 44 having a plurality of driver circuit output terminals,

a driver circuit output terminal of said a plurality of driver circuit output terminals providing a signal potential to a signal line of said plurality of signal lines (specification at page 19, lines 5-6),

the quantity of said driver circuit output terminals being the same quantity for said each of said plurality of driver circuits 14, 44 (specification at figure 6), and

the quantity of said driver circuits 14, 44 being defined as N/n, wherein "N" is the quantity of said signal lines and "n" is said quantity of said driver circuit output terminals (specification at page 44, lines 23-26).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issues presented for consideration in this appeal are as follows:

Whether the Examiner erred in paragraphs 8-44 by rejecting claims 25-29, 31, 37, 43-48, and 67-78 under 35 U.S.C. §112, second paragraph.

Whether the Examiner erred in paragraph 48 by rejecting claims 25-29, 31, 37, 43-48, and 71-78 under 35 U.S.C. 102 as allegedly being anticipated by U.S. Patent No. 4,825,203 (Takeda).

Whether the Examiner erred in paragraph 49 by rejecting claims 25-29, 31, 37, 43-48, and 71-78 under 35 U.S.C. 102 as allegedly being anticipated by U.S. Patent No. 5,440,304 (Hirai).

Whether the Examiner erred in paragraph 50 by rejecting claims 25-29, 31, 37, 43-48, and 71-78 under 35 U.S.C. 103 as allegedly being unpatentable over U.S. Patent No. 4,825,203 (Takeda) in view of U.S. Patent No. 5,440,304 (Hirai).

Whether the Examiner erred in paragraph 51 by rejecting claims 49-66 under 35 U.S.C. 103 as allegedly being unpatentable over U.S. Patent No. 4,825,203 (Takeda) in view of U.S. Patent No. 5,426,447 (Lee).

Whether the Examiner erred in paragraph 52 by rejecting claims 67-70 under 35 U.S.C. 103 as allegedly being unpatentable over U.S. Patent No. 4,825,203 (Takeda) in view of U.S. Patent No. 5,426,447 (Lee), and in further view of U.S. Patent No. 5,440,304 (Hirai).

Whether the Examiner erred in paragraph 54 by rejecting claim 49 under 35 U.S.C. 102 as allegedly being anticipated by U.S. Patent No. 4,745,406 (Hayashi).

Whether the Examiner erred in paragraph 55 by rejecting claims 67-70 under 35 U.S.C. 103 as allegedly being unpatentable over U.S. Patent No. 4,745,406 (Hayashi) in view of U.S. Patent No. 5,440,304 (Hirai).

Whether the Examiner erred in paragraph 56 by rejecting claims 67-70 under 35 U.S.C. 102 as allegedly being anticipated by U.S. Patent No. 5,440,304 (Hirai).

These issues will be discussed hereinbelow.

VII. ARGUMENT

In the Office Action of May 28, 2008:

In paragraphs 8-44 of the Office Action, the Examiner indicated a rejection of claims 25-29, 31, 37, 43-48, and 67-78 under 35 U.S.C. §112, second paragraph.

In paragraph 48 of the Office Action, the Examiner indicated a rejection of claims 25-29, 31, 37, 43-48, and 71-78 under 35 U.S.C. 102 as allegedly being anticipated by U.S. Patent No. 4,825,203 (Takeda).

In paragraph 49 of the Office Action, the Examiner indicated a rejection of claims 25-29, 31, 37, 43-48, and 71-78 under 35 U.S.C. 102 as allegedly being anticipated by U.S. Patent No. 5,440,304 (Hirai).

In paragraph 50 of the Office Action, the Examiner indicated a rejection of claims 25-29, 31, 37, 43-48, and 71-78 under 35 U.S.C. 103 as allegedly being unpatentable over U.S. Patent No. 4,825,203 (Takeda) in view of U.S. Patent No. 5,440,304 (Hirai).

In paragraph 51 of the Office Action, the Examiner indicated a rejection of claims 49-66 under 35 U.S.C. 103 as allegedly being unpatentable over U.S. Patent No. 4,825,203 (Takeda) in view of U.S. Patent No. 5,426,447 (Lee).

In paragraph 52 of the Office Action, the Examiner indicated a rejection of claims 67-70 under 35 U.S.C. 103 as allegedly being unpatentable over U.S. Patent No. 4,825,203 (Takeda) in view of U.S. Patent No. 5,426,447 (Lee), and in further view of U.S. Patent No. 5,440,304 (Hirai).

In paragraph 54 of the Office Action, the Examiner indicated a rejection of claim 49 under 35 U.S.C. 102 as allegedly being anticipated by U.S. Patent No. 4,745,406 (Hayashi).

In paragraph 55 of the Office Action, the Examiner indicated a rejection of claims 67-70 under 35 U.S.C. 103 as allegedly being unpatentable over U.S. Patent No. 4,745,406 (Hayashi) in view of U.S. Patent No. 5,440,304 (Hirai).

In paragraph 56 of the Office Action, the Examiner indicated a rejection of claims 67-70 under 35 U.S.C. 102 as allegedly being anticipated by U.S. Patent No. 5,440,304 (Hirai).

In paragraph 57 of the Office Action, the Examiner indicated a rejection of claims 67-70 under 35 U.S.C. 103 as allegedly being unpatentable over U.S. Patent No. 5,440,304 (Hirai).

For at least the following reasons, Appellant submits that this rejection is both technically and legally unsound and should therefore be reversed.

For purposes of this appeal brief only, and without conceding the teachings of any prior art reference, the claims have been grouped as indicated below.

The Examiner erred in paragraphs 8-44 by rejecting claims 25-29, 31, 37, 43-48, and 67-78 under 35 U.S.C. §112, second paragraph.

This rejection is traversed at least for the following reasons.

Claim 25 is drawn to a liquid crystal display comprising:

A DISPLAY PORTION, said display portion having a plurality of gate lines, ***A PLURALITY OF SIGNAL LINES*** and a plurality of pixels,

a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and

A PLURALITY OF DRIVER CIRCUITS, said plurality of driver circuits including ***AT LEAST ONE GENERAL DRIVER CIRCUIT*** and ***ONE REMAINDER DRIVER CIRCUIT***,

EACH SAID AT LEAST ONE GENERAL DRIVER CIRCUIT having ***A GENERAL DRIVER HORIZONTAL SHIFT REGISTER CIRCUIT*** and a plurality of general driver circuit output terminals, a general driver circuit output terminal of said plurality of general driver circuit output terminals providing a signal potential to one of said plurality of signal lines,

said remainder driver circuit having ***A REMAINDER DRIVER HORIZONTAL SHIFT REGISTER CIRCUIT*** and ***A PLURALITY OF REMAINDER DRIVER CIRCUIT OUTPUT TERMINALS***, a remainder driver circuit output terminal of said plurality of remainder driver circuit output terminals providing ***ANOTHER SIGNAL POTENTIAL*** to ***ANOTHER OF SAID PLURALITY OF SIGNAL LINES***,

the quantity of said remainder driver circuit output terminals being defined as (S – (OP * (DC-1))), "S" being the quantity of said plurality of signal lines, "OP" being the quantity of said general driver circuit output terminals, and "DC" being the quantity of said plurality of driver circuits, and

said quantity of said general driver circuit output terminals being different than said quantity of said remainder driver circuit output terminals.

As shown by the uppercase lettering, the a proper antecedent basis has been established within claim 25.

Claim 26 is drawn to a display according to claim 25, wherein one driver circuit of ***said plurality of driver circuits*** is separate and distinct from another driver circuit of said plurality of driver circuits.

As shown by the uppercase lettering, the a proper antecedent basis for the terms found within claim 26 has been established within claim 25.

Claim 28 is drawn to a display according to claim 25, wherein said pixel of said plurality of pixels includes a transistor, a gate electrode of said transistor being electrically connected to said gate line, ***A SOURCE/DRAIN OF SAID TRANSISTOR*** being electrically connected to said signal line.

As a rule, the ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application. *Phillips v. AWH Corp.*, 75 USPQ2d 1321, 1326 (Fed. Cir. 2005).

Here, the term "source/drain" is standard terminology within the semiconductor art and its meaning is readily understood by the skilled artisan.

Claim 31 is drawn to a display according to claim 25, wherein ***A SURPLUS CONNECTING REGION*** that *does not contribute* to said display portion does not occur on the said display.

For claim construction purposes, the description may act as a sort of dictionary, which explains the invention and may define terms used in the claims." *General Electric Co. v. Nintendo Co.*, 50 USPQ2d 1910, 1914 (Fed. Cir. 1999).

Attention is drawn to specification page 16, lines 22-24.

Claim 37 is drawn to a display according to claim 25, wherein an output terminal of *said plurality of driver circuits* is electrically connected to an input terminal of a time-divisional switch, said time-divisional switch providing a de-multiplexed signal potential to said signal line, said de-multiplexed signal potential being a signal potential for one of ***A PLURALITY OF PRIMARY COLORS*** that is time-divided from another signal potential for another of said plurality of primary colors and supplied to said signal line.

As shown by the uppercase lettering, the a proper antecedent basis for the terms found within claim 37 has been established within claim 25.

Claim 43 is drawn to a display according to claim 37, wherein *said plurality of primary colors* is a first primary color, a second primary color and ***A THIRD PRIMARY COLOR***.

Claim 37 provides for a ***plurality*** of primary colors. As shown by the uppercase lettering, the a proper antecedent basis for the terms found within claim 43 has been established within claim 37.

Claim 45 is drawn to a display according to claim 25, wherein ***THE SUM TOTAL OF GENERAL DRIVER CIRCUIT OUTPUT TERMINALS*** and *said remainder driver circuit output terminals* is equal to *said plurality of signal lines*.

As shown by the uppercase lettering, the a proper antecedent basis for the terms found within claim 45 has been established within claims 25 and 45.

Claim 46 is drawn to a display according to claim 25, wherein *said plurality of driver circuits* includes more than one *said general driver circuit*.

As shown by the uppercase lettering, the a proper antecedent basis for the terms found within claim 46 has been established within claim 25.

Claim 47 is drawn to a display according to claim 46, wherein *said each said at least one general driver circuit* has ***AN EQUAL NUMBER OF GENERAL DRIVER CIRCUIT OUTPUT TERMINALS***.

As shown by the uppercase lettering, the a proper antecedent basis for the terms found within claim 47 has been established within claims 25 and 47.

Claim 48 is drawn to a display according to claim 25, wherein *said plurality of driver circuits* are driver integrated circuits arranged in an outside of a transparent insulating substrate on which *said display portion* is formed.

As shown by the uppercase lettering, the a proper antecedent basis for the terms found within claim 48 has been established within claim 25.

Claim 49 is drawn to a liquid crystal display comprising:

A DISPLAY PORTION, said display portion having a plurality of gate lines, a plurality of signal lines and a plurality of pixels,

a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and

A PLURALITY OF DRIVER CIRCUITS, ***EACH OF SAID PLURALITY OF DRIVER CIRCUITS*** having a plurality of driver circuit output terminals,

a driver circuit output terminal of said a plurality of driver circuit output terminals providing a signal potential to a signal line of said plurality of signal lines,

the quantity of said driver circuit output terminals being the same quantity for said each of said plurality of driver circuits, and

the quantity of said driver circuits being defined as N/n, wherein "N" is the quantity of said signal lines and "n" is said quantity of said driver circuit output terminals.

Claim 67 is drawn to a display according to claim 49, wherein *said each of said plurality of driver circuits* has ***A HORIZONTAL SHIFT REGISTER CIRCUIT***.

As shown by the uppercase lettering, the a proper antecedent basis for the terms found within claim 68 has been established within claims 49 and 67.

In addition, for claim construction purposes, the description may act as a sort of dictionary, which explains the invention and may define terms used in the claims." *General Electric Co. v. Nintendo Co.,* 50 USPQ2d 1910, 1914 (Fed. Cir. 1999).

Attention is drawn to specification page 11, line 26 to page 12, line 1.

Claim 68 is drawn to a display according to claim 67, wherein ***ONE GENERAL DRIVER HORIZONTAL SHIFT REGISTER CIRCUIT*** of *said plurality of driver circuits* is separate and distinct from ***ANOTHER GENERAL DRIVER HORIZONTAL SHIFT REGISTER CIRCUIT*** of *said plurality of driver circuits*.

As shown by the uppercase lettering, the a proper antecedent basis for the terms found within claim 68 has been established within claims 49 and 68.

Moreover, attention is drawn to specification page 11, line 26 to page 12, line 1.

Claim 69 is drawn to a display according to claim 67, wherein *said horizontal shift register circuit* performs ***A HORIZONTAL SCAN*** by sequentially generating ***HORIZONTAL SCANNING PULSES***.

As shown by the uppercase lettering, the a proper antecedent basis for the terms found within claim 69 has been established within claims 67 and 69.

Moreover, attention is drawn to specification page 11, line 26 to page 12, line 15.

Claim 70 is drawn to a display according to claim 67, wherein *said horizontal shift register circuit* has sampling switches, a level shifter, a data latch circuit, and ***A DIGITAL/ANALOG CONVERTING CIRCUIT***.

Attention is drawn to specification figure 4 and page 11, line 24 to page 12, line 7.

Claim 71 is drawn to a display according to claim 25, wherein ***ONE GENERAL DRIVER HORIZONTAL SHIFT REGISTER CIRCUIT*** of *said plurality of driver circuits* is separate and distinct from ***ANOTHER GENERAL DRIVER HORIZONTAL SHIFT REGISTER CIRCUIT*** of *said plurality of driver circuits*.

As shown by the uppercase lettering, the a proper antecedent basis for the terms found within claim 71 has been established within claims 25 and 71.

Moreover, attention is drawn to specification page 11, line 26 to page 12, line 1.

Claim 72 is drawn to a display according to claim 25, wherein *said general driver horizontal shift register* circuit performs ***A HORIZONTAL SCAN*** by sequentially generating ***HORIZONTAL SCANNING PULSES***.

As shown by the uppercase lettering, the a proper antecedent basis for the terms found within claim 72 has been established within claims 25 and 72.

Moreover, attention is drawn to specification page 11, line 26 to page 12, line 15.

Claim 73 is drawn to a display according to claim 25, wherein *said each said at least one general driver circuit* has ***GENERAL DRIVER SAMPLING SWITCHES***, a general driver level shifter, a general driver data latch circuit, and ***A GENERAL DRIVER DIGITAL/ANALOG CONVERTING CIRCUIT***.

Attention is drawn to specification figure 4 and page 11, line 24 to page 12, line 7.

Claim 74 is drawn to a display according to claim 73, wherein ***SAMPLING SWITCHES*** in *said general driver sampling switches* sequentially sample ***INPUT DIGITAL IMAGE DATA*** in response to horizontal scanning pulses from said general driver horizontal shift register circuit.

Attention is drawn to specification figure 4 and page 11, line 24 to page 12, line 15.

Claim 75 is drawn to a display according to claim 73, wherein *said general driver level shifter* boosts ***DIGITAL DATA*** sampled by said general driver sampling switches to digital data of a liquid crystal driving voltage.

Attention is drawn to specification figure 4 and page 11, line 24 to page 12, line 15.

Claim 76 is drawn to a display according to claim 73, wherein said general driver data latch circuit is a memory to accumulate ***DIGITAL DATA*** boosted by said general driver level shifter by an amount of one horizontal period.

Attention is drawn to specification figure 4 and page 11, line 24 to page 12, line 24.

Claim 77 is drawn to a display according to claim 73, wherein *said general driver digital/analog converting circuit* converts ***DIGITAL DATA*** of one horizontal period which is outputted from said general driver data latch circuit into an analog signal and outputs said analog signal.

Attention is drawn to specification figure 4 and page 11, line 24 to page 12, line 15.

Claim 78 is drawn to a display according to claim 73, wherein said remainder driver circuit has remainder driver sampling switches, a remainder driver level shifter, a remainder driver data latch circuit, and ***A REMAINDER DRIVER DIGITAL/ANALOG CONVERTING CIRCUIT***.

Attention is drawn to specification figure 4 and page 11, line 24 to page 12, line 7.

Thus, it is believed that the metes and bounds of what is being claimed within the claims can be readily ascertained by those of ordinary skill in the art.

The Examiner erred in paragraph 48 by rejecting claims 25-29, 31, 37, 43-48, and 71-78 under 35 U.S.C. 102 as allegedly being anticipated by U.S. Patent No. 4,825,203 (Takeda).

The Examiner erred in paragraph 49 by rejecting claims 25-29, 31, 37, 43-48, and 71-78 under 35 U.S.C. 102 as allegedly being anticipated by U.S. Patent No. 5,440,304 (Hirai).

The Examiner erred in paragraph 50 by rejecting claims 25-29, 31, 37, 43-48, and 71-78 under 35 U.S.C. 103 as allegedly being unpatentable over U.S. Patent No. 4,825,203 (Takeda) in view of U.S. Patent No. 5,440,304 (Hirai).

These rejections are traversed at least for the following reasons.

Claims 25-29, 31, 37, 43-47, 71-78 stand or fall together - Claims 25-29, 31, 37, 43-47 are dependent upon claim 25. Claim 25 includes the features of:

> a display portion 10 (specification at figure 5), said display portion 10 having a plurality of gate lines 11, a plurality of signal lines 12 and a plurality of pixels 20 (specification at figure 3, page 9, lines 5-17),
>
> a pixel 20 of said plurality of pixels 20 being located at an intersection of a gate line 11 of said plurality of gate lines 11 and a signal line 12 of said plurality of signal lines 12 (specification at figure 3); and
>
> a plurality of driver circuits 14, 44 (specification at page 19, lines 5-6), said plurality of driver circuits 14, 44 including at least one general driver circuit and one remainder driver circuit (specification at figure 5),
>
> each said at least one general driver circuit 14, 44 having a general driver horizontal shift register circuit 31 (specification at figure 4, page 11, line 26 to page 12, line 1) and a plurality of general driver circuit output terminals, a general driver circuit output terminal of said plurality of general driver circuit output terminals providing a

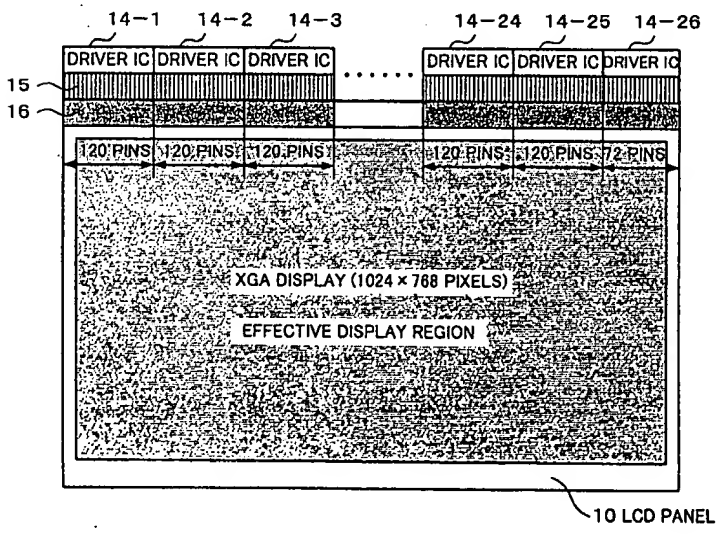
signal potential to one of said plurality of signal lines (specification at page 19, lines 5-6),

said remainder driver circuit having a remainder driver horizontal shift register circuit 31 (specification at figure 4, page 11, line 26 to page 12, line 1) and a plurality of remainder driver circuit output terminals, a remainder driver circuit output terminal of said plurality of remainder driver circuit output terminals providing another signal potential to another of said plurality of signal lines (specification at figure 5),

the quantity of remainder driver circuit output terminals being defined as (S – (OP * (DC-1))) (specification at figure 5, page 13, lines 18-21), "S" being the quantity of said plurality of signal lines 12 (specification at page 13, lines 10-13), "OP" being the quantity of general driver circuit output terminals, and "DC" being the quantity of said plurality of driver circuits 14 (specification at figure 5, page 13, lines 21-26),

said quantity of general driver circuit output terminals being different than said quantity of remainder driver circuit output terminals (specification at figure 5).

Figure 5 of the specification as originally filed is provided hereinbelow.



Takeda - The Office Action at pages 24-25 contends that Takeda discloses the presence of the following:

a display portion 11 (Figure 2);

gate lines 11-a (Figure 2);

signal lines 11-b (Figure 2);

pixels 11-c (Figure 2);

at least one general driver circuit q_1, q_2, q_3 (Figures 1(A), 2);

one remainder driver circuit q_{N-1}, q_N (Figure 1(A));

a general driver horizontal shift register circuit 31 (Figure 1(A));

a remainder driver horizontal shift register circuit 31 (Figure 1(A)).

The express teachings of Takada are clear and unmistakable. Here, Figure 2 of Takada shows the presence of a ***single*** column electrode ***drive circuit*** 13. As explained, *numeral (13)* is the *column electrode **drive circuit*** which applies the display signal that includes the color signal to the column electrode line, synchronized with the scanning pulse applied to the row electrode line (Takada at column 3, lines 4-8).

Whereas claim 25 provides for the presence of ***a PLURALITY of driver circuits 14*** as shown hereinabove within Figure 5 of the specification as originally filed, only one column electrode drive circuit 13 is depicted within Figure 2 of Takeda.

Figures 1(A) and 2 of Takeda are provided hereinbelow.

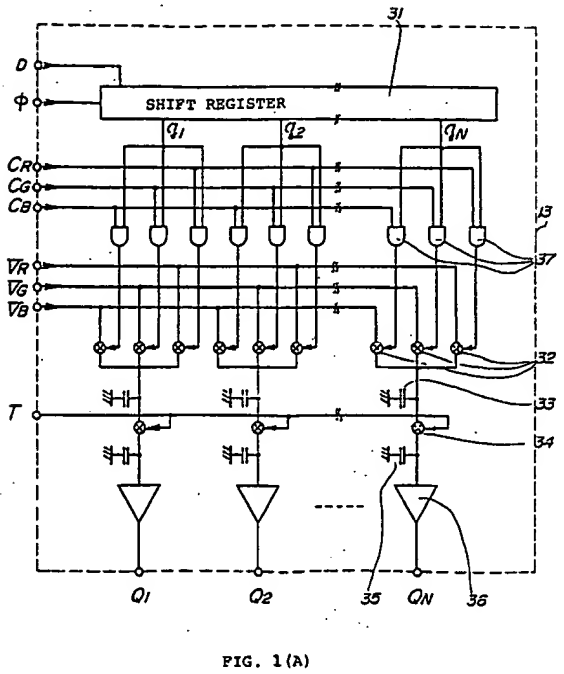
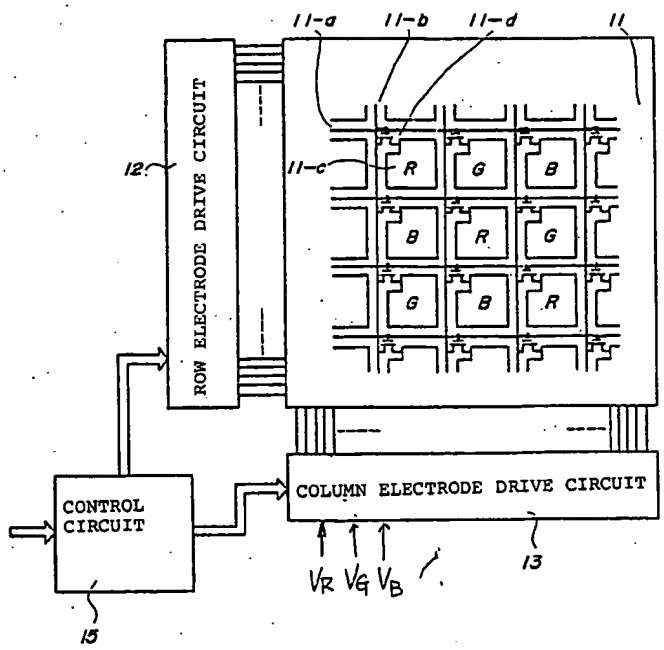


FIG. 1(A)

FIG. 2



Nevertheless, the Office Action at page 24 refers to Figure 1(A) for the teaching of a *plurality* of driver circuits notwithstanding the express teachings found within Takada.

Specifically, the Office Action at pages 24-25 contends that Figure 1(A) of Takeda discloses the presence of at least one general driver circuit q_1, q_2, q_3 and one remainder driver circuit q_{N-1}, q_N.

As an initial matter, while Takada may quite possibly teach elements q_1 through q_N as being a signal corresponding to the display pattern to each column electrode line that is output from shift register (31) (Takada at column 4, lines 29-31), Takeda ***fails*** to disclose, teach or suggest elements q_1 through q_N as being a circuit.

Moreover, Takada ***fails*** to disclose Figures 1 (A), (B) as depicting a ***plurality*** of driver circuits 13.

Instead, Figures 1 (A), (B) is a diagram showing ***the configuration of the column electrode drive circuit (13)*** in the drive circuit of the liquid crystal display device to explain an embodiment of this invention and a timing waveform chart showing the voltage waveforms of the major components of ***the column electrode drive circuit (13)*** (Takeda at column 4, lines 22-28).

But even if Figure 1(A) of Takeda discloses the presence of at least one general driver circuit q_1, q_2, q_3 and one remainder driver circuit q_{N-1}, q_N as the Office Action contends, Takada ***fails*** to disclose an output terminal for any of the alleged driver circuits q_1 through q_N as providing a signal potential to any of the column electrodes 11-b.

Instead, the skilled artisan would have readily appreciated in Takeda that the ***output from the gate circuit (37)*** connected to the output end of the shift register to changeover color ***is input to the sampling analog switch (32)*** to enable selection of one of the three selection signals with the sampling analog switch (32) (Takeda at column 4, lines 38-43).

Furthermore, the selection signals CR CG, CB are simultaneously input to the gate circuit (37), therefore ***the signals output from the gate circuit (37) sample the display signal (VR, VG or VB)*** corresponding to the column electrode through the sampling analog switch (32), which is stored in the sampling condensor (33) (Takeda at column 4, lines 63-67).

As a consequence, Takeda ***fails*** to teach that the output from the gate circuit (37) found within Figure 1(A) of Takeda is connected to any of the column electrodes 11-b found within Figure 2 of Takeda.

- ***Thus, Takeda fails to disclose, teach, or suggest a plurality of driver circuits, said plurality of driver circuits including at least one general driver circuit and one remainder driver circuit.***

Regarding the feature of either a general driver horizontal shift register circuit or a remainder driver horizontal shift register circuit, Takada ***fails*** to disclose any of the alleged driver circuits q_1 through q_N as having a shift register.

Instead, the column electrode drive circuit mainly comprises a shift register (31) which outputs a signal corresponding to the display pattern to each column electrode line, analog switches (32), (34), condensors (33), (35) and an output buffer (36) (Takeda at column 4, lines 29-33).

- ***Thus, Takeda fails to disclose, teach, or suggest each said at least one general driver circuit having a general driver horizontal shift register circuit and a plurality of general driver circuit output terminals, a general driver circuit output terminal of said plurality of general driver circuit output terminals providing a signal potential to one of said plurality of signal lines.***

- ***Furthermore, Takeda fails to disclose, teach, or suggest said remainder driver circuit having a remainder driver horizontal shift register circuit and a plurality of remainder driver circuit output terminals, a remainder driver circuit output terminal of said plurality of remainder driver circuit output terminals providing another signal potential to another of said plurality of signal lines.***

The Final Office Action asserts without provided any evidentiary support that there are two (2) remainder driver circuit output terminals, five (5) plurality of signal lines, three (3) general driver circuit output terminals, and two (2) plurality of driver circuits.

In response, this unsupported assertion amounts to nothing more than conclusions that are personal in nature because the cited prior art does not contain a sufficient teaching of how to obtain the desired result, or that the claimed result would be obtained if certain directions were pursued. In this regard, the teachings, suggestions or incentives supporting the rejection must be clear and particular.

- ***Thus, Takeda fails to disclose, teach, or suggest the quantity of said remainder driver circuit output terminals being defined as (S – (OP * (DC-1))), "S" being the quantity of said plurality of signal lines, "OP" being the quantity of said general driver circuit output terminals, and "DC" being the quantity of said plurality of driver circuits, and***

said quantity of said general driver circuit output terminals being different than said quantity of said remainder driver circuit output terminals.

Hirai - The Office Action applies Hirai individually or for the features that are deficient from within Takada.

Figure 3 shows an example of a liquid crystal device driving integrated circuit (IC) (Hirai at column 1, lines 10-11).

Figure 3 of Hirai is provided hereinbelow.

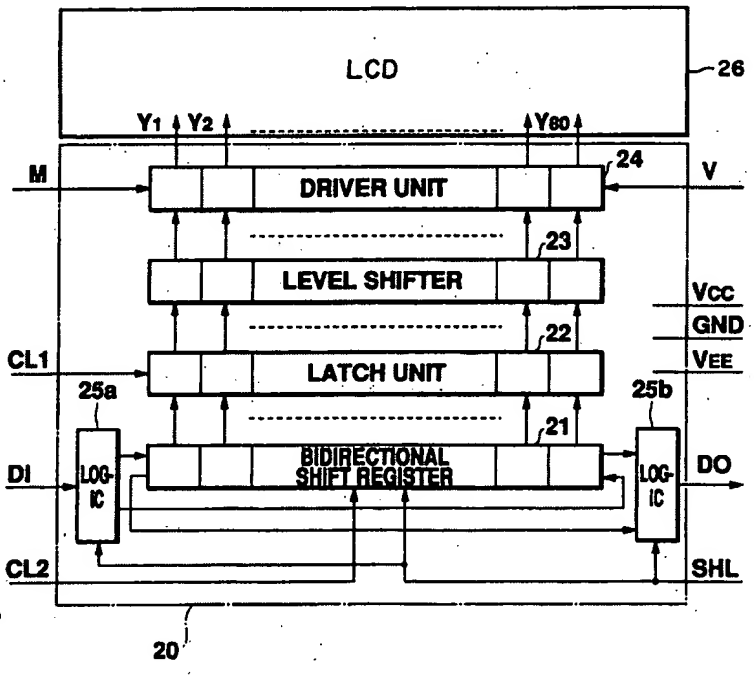


FIG. 3
(PRIOR ART)

Figure 3 of Hirai and Figure 2 of Takeda may reveal, quite possibly, a similarity between element 20 of Hirai and element 13 of Takeda.

In this regard, Figures 4 and 5 of Hirai are provided hereinbelow.

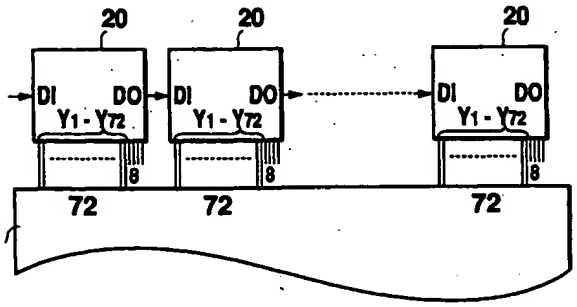


FIG. 4
(PRIOR ART)

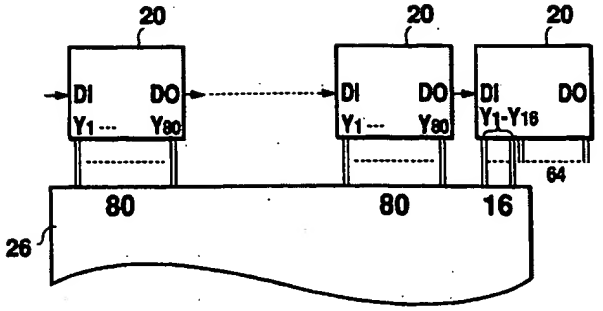


FIG. 5
(PRIOR ART)

Method A requires the circuit configuration as shown in Figure 4, for example (Hirai at column 2, lines 5-6). For method A, because 72 × 8=576, each of ***eight ICs 20*** may be used as a 72-bit output IC without using output pins $Y_{73\text{-}80}$ (eight bits) of each IC 20. (Hirai at column 2, lines 8-10).

Method B requires the circuit configuration as shown in Figure 5, for example (Hirai at column 2, lines 6-7). On the other hand, for method B, because 80 × 7 +16=576, all of ***seven ICs 20*** may be used 80-bit output ICs with the eighth IC 20 as a 16-bit output IC (Hirai at column 2, lines 10-13).

To display a character made up of 16 × 16=256 dots, if method A is used, each of four ICs 20 may be used as a 64-bit output IC; if method B is used, three ICs 20 may be used as 80-bit output ICs with the fourth device of IC 20 as a 16-bit output IC (Hirai at column 2, lines 14-18).

Likewise, to display a character made up of 32 × 32=1024 dots, if method A is used, sixteen ICs 20 may be used as 64-bit output ICs; if method B is used, twelve ICs 20 are used as 80-bit output ICs and eleven ICs 20 are used as 64-bit output ICs (Hirai at column 2, lines 18-23).

Further, to display a character made up of 48 × 48=2304 dots, if method A is used, thirty-two ICs 20 are used as 72-bit output ICs; if method B is used, twenty-eight ICs 20 are used as 80-bit output ICs and one IC 20 is used as a 64-bit output IC (Hirai at column 2, lines 24-28).

- ***However, Hirai fails to disclose, teach, or suggest the quantity of said remainder driver circuit output terminals being defined as (S – (OP * (DC-1))), "S" being the quantity of said plurality of signal lines, "OP" being the quantity of said general driver circuit output terminals, and "DC" being the quantity of said plurality of driver circuits, and said quantity of said general driver circuit output terminals being different than said quantity of said remainder driver circuit output terminals.***

Claim 48 stands or falls alone - Claim 48 is dependent upon claim 25. Claim 48 includes the features of a display according to claim 25, wherein said plurality of driver circuits are driver integrated circuits arranged in an outside of a ***transparent insulating substrate*** on which said display portion is formed.

However, Takeda and Hirai, either individually or as a whole, ***fail*** to disclose, teach or suggest the presence of ***a transparent insulating substrate***.

The Examiner erred in paragraph 51 by rejecting claims 49-66 under 35 U.S.C. 103 as allegedly being unpatentable over U.S. Patent No. 4,825,203 (Takeda) in view of U.S. Patent No. 5,426,447 (Lee).

The Examiner erred in paragraph 52 by rejecting claims 67-70 under 35 U.S.C. 103 as allegedly being unpatentable over U.S. Patent No. 4,825,203 (Takeda) in view of U.S. Patent No. 5,426,447 (Lee), and in further view of U.S. Patent No. 5,440,304 (Hirai).

The Examiner erred in paragraph 54 by rejecting claim 49 under 35 U.S.C. 102 as allegedly being anticipated by U.S. Patent No. 4,745,406 (Hayashi).

The Examiner erred in paragraph 55 by rejecting claims 67-70 under 35 U.S.C. 103 as allegedly being unpatentable over U.S. Patent No. 4,745,406 (Hayashi) in view of U.S. Patent No. 5,440,304 (Hirai).

The Examiner erred in paragraph 56 by rejecting claims 67-70 under 35 U.S.C. 102 as allegedly being anticipated by U.S. Patent No. 5,440,304 (Hirai).

The Examiner erred in paragraph 56 by rejecting claims 67-70 under 35 U.S.C. 103 as allegedly being unpatentable over U.S. Patent No. 5,440,304 (Hirai).

These rejections are traversed at least for the following reasons.

Claims 49-70 stand or fall together - Claims 50-70 are dependent upon claim 49. Claim 49 is drawn to a liquid crystal display comprising:

> a display portion 10 (specification at Figure 6), said display portion 10 having a plurality of gate lines 11, a plurality of signal lines 12 and a plurality of pixels 20 (specification at figure 3, page 9, lines 5-17),

a pixel 20 of said plurality of pixels 20 being located at an intersection of a gate line 11 of said plurality of gate lines 11 and a signal line 12 of said plurality of signal lines 12 (specification at figure 3), and

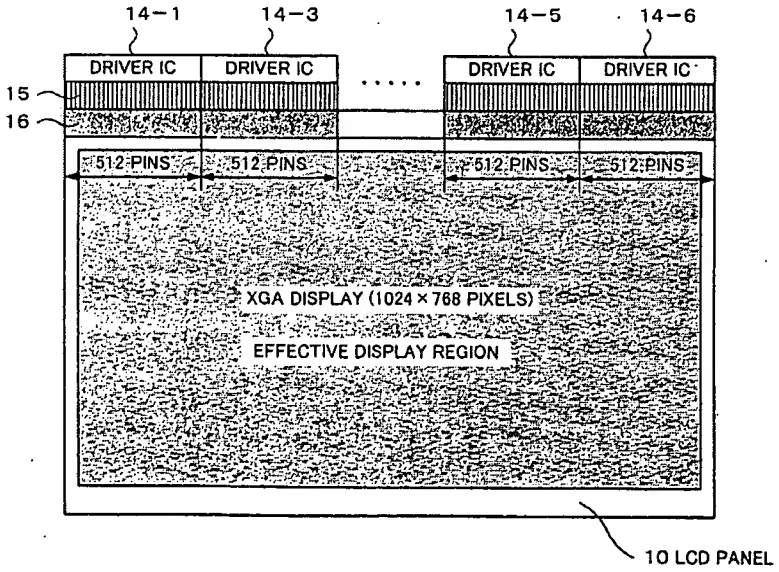
a plurality of driver circuits 14, 44, each of said plurality of driver circuits 14, 44 having a plurality of driver circuit output terminals,

a driver circuit output terminal of said a plurality of driver circuit output terminals providing a signal potential to a signal line of said plurality of signal lines (specification at page 19, lines 5-6),

the quantity of said driver circuit output terminals being the same quantity for said each of said plurality of driver circuits 14, 44 (specification at figure 6), and

the quantity of said driver circuits 14, 44 being defined as N/n, wherein "N" is the quantity of said signal lines and "n" is said quantity of said driver circuit output terminals (specification at page 44, lines 23-26).

Figure 6 of the specification as originally filed is provided hereinbelow.



Takeda - The Office Action at pages 38-39 contends that Takeda discloses the presence of the following:

a display portion 11 (Figure 2);

gate lines 11-a (Figure 2);

signal lines 11-b (Figure 2);

pixels 11-c (Figure 2);

at least one general driver circuit q_1, q_2, q_3 (Figures 1(A), 2);

one remainder driver circuit q_{N-1}, q_N (Figure 1(A));

a general driver horizontal shift register circuit 31 (Figure 1(A));

a remainder driver horizontal shift register circuit 31 (Figure 1(A)).

Figures 1(A) and 2 of Takeda are provided hereinbelow.

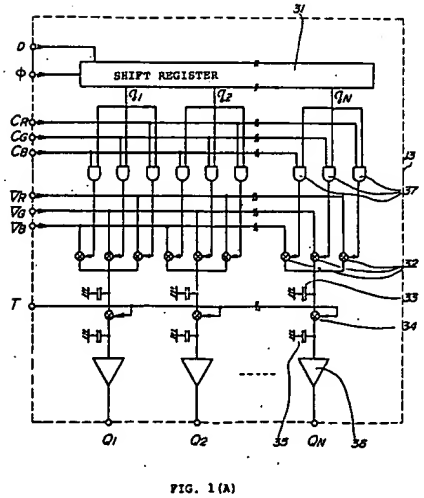
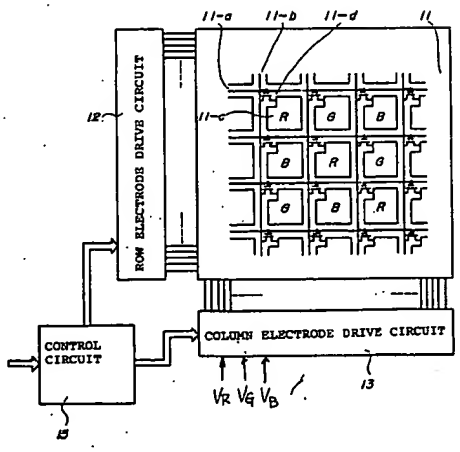


FIG. 1(A)

FIG. 2



The express teachings of Takada are clear and unmistakable. Here, Figure 2 of Takada shows the presence of a ***single*** column electrode ***drive circuit*** 13. As explained, *numeral (13)* is the *column electrode* ***drive circuit*** which applies the display signal that includes the color signal to the column electrode line, synchronized with the scanning pulse applied to the row electrode line (Takada at column 3, lines 4-8).

Whereas claim 25 provides for the presence of ***a PLURALITY of driver circuits 14*** as shown hereinabove within Figure 5 of the specification as originally filed, only one column electrode drive circuit 13 is depicted within Figure 2 of Takeda.

Nevertheless, the Office Action at page 24 refers to Figure 1(A) for the teaching of a *plurality* of driver circuits notwithstanding the express teachings found within Takada. Specifically, the Office Action at pages 24-25 contends that Figure 1(A) of Takeda discloses the presence of at least one general driver circuit q_1, q_2, q_3 and one remainder driver circuit q_{N-1}, q_N.

As an initial matter, while Takada may quite possibly teach elements q_1 through q_N as being a signal corresponding to the display pattern to each column electrode line that is output from shift register (31) (Takada at column 4, lines 29-31), Takeda ***fails*** to disclose, teach or suggest elements q_1 through q_N as being a circuit.

Moreover, Figures 1 (A), (B) is a diagram showing ***the configuration of the column electrode drive circuit (13)*** in the drive circuit of the liquid crystal display device to explain an embodiment of this invention and a timing waveform chart showing the voltage waveforms of the major components of ***the column electrode drive circuit (13)*** (Takeda at column 4, lines 22-28).

However, Takada ***fails*** to disclose Figures 1 (A), (B) as depicting a ***plurality*** of driver circuits 13.

But even if Figure 1(A) of Takeda discloses the presence of at least one general driver circuit q_1, q_2, q_3 and one remainder driver circuit q_{N-1}, q_N as the Office Action contends, Takada

fails to disclose an output terminal for any of the alleged driver circuits q_1 through q_N as providing a signal potential to any of the column electrodes 11-b.

Instead, the skilled artisan would have readily appreciated in Takeda that the ***output from the gate circuit (37)*** connected to the output end of the shift register to changeover color ***is input to the sampling analog switch (32)*** to enable selection of one of the three selection signals with the sampling analog switch (32) (Takeda at column 4, lines 38-43).

Furthermore, the selection signals CR CG, CB are simultaneously input to the gate circuit (37), therefore ***the signals output from the gate circuit (37) sample the display signal (VR, VG or VB)*** corresponding to the column electrode through the sampling analog switch (32), which is stored in the sampling condensor (33) (Takeda at column 4, lines 63-67).

As a consequence, Takeda ***fails*** to teach that the output from the gate circuit (37) found within Figure 1(A) of Takeda is connected to any of the column electrodes 11-b found within Figure 2 of Takeda.

- ***Thus, Takeda fails to disclose, teach, or suggest a plurality of driver circuits, said plurality of driver circuits including at least one general driver circuit and one remainder driver circuit.***

- ***Moreover, Takeda fails to disclose, teach, or suggest the quantity of said driver circuit output terminals being the same quantity for said each of said plurality of driver circuits.***

- ***Finally, Takeda fails to disclose, teach, or suggest the quantity of said driver circuits being defined as N/n, wherein "N" is the quantity of said signal lines and "n" is said quantity of said driver circuit output terminals.***

Lee - The Office Action applies Lee individually or for the features that are deficient from within Takada.

Lee arguably teaches that Figure 1 is a basic block diagram of the novel display system 10 which includes the display device 14 and the "off-glass" control circuits 12 that are separate from and connected to the display 14 to drive the elements thereon (Lee at column 4, lines 22-26).

Figure 1 of Lee is provided hereinbelow.

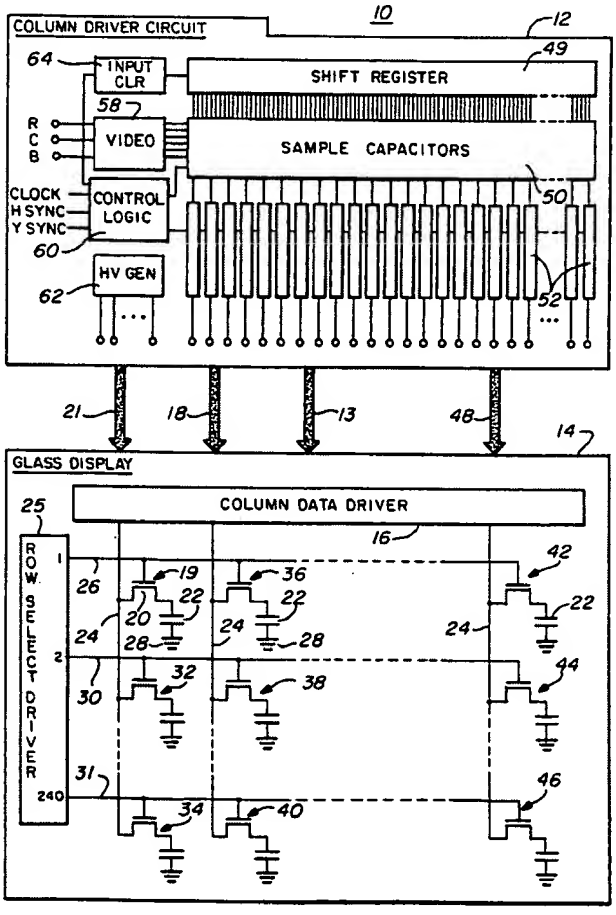


FIG. 1

Figure 1 of Lee and Figure 2 of Takeda may reveal, quite possibly, a similarity between element 12 of Lee and element 13 of Takeda.

Thus, if one row of pixels includes 384 display elements, the 64 ***data input lines 13*** are coupled in multiplexed fashion, 64 bits at a time, to the 384 display elements on the substrate 14 (Lee at column 4, lines 57-60).

On ***line 18***, from control circuit 12, six pairs of video select signal lines are applied to the column data drivers 16 on glass 14 to demultiplex the 64 output signals and couple them sequentially to X (6) different groups of Y (64) columns 24 in a selected one of Z (240) rows on the glass 14 (Lee at column 4, lines 63-68).

The row select driver signals, the clock and power lines are coupled from the control circuit 12 on ***line 21*** to the row select driver circuit 25 as will be shown hereafter (Lee at column 4, line 68 to column 5, line 3).

Row select driver circuit 25 may be any of such type of circuits well known in the art. Precharge signals are coupled on ***line 48*** to substrate 14 (Lee at column 5, lines 3-5).

- ***However, Lee fails to disclose, teach, or suggest a plurality of driver circuits, said plurality of driver circuits including at least one general driver circuit and one remainder driver circuit.***

- ***Moreover, Lee fails to disclose, teach, or suggest the quantity of said driver circuit output terminals being the same quantity for said each of said plurality of driver circuits.***

- ***Finally, Lee fails to disclose, teach, or suggest the quantity of said driver circuits being defined as N/n, wherein "N" is the quantity of said signal lines and "n" is said quantity of said driver circuit output terminals.***

Hirai - The Office Action applies Hirai individually or for the features that are deficient from within Takada.

Figure 3 shows an example of a liquid crystal device driving integrated circuit (IC) (Hirai at column 1, lines 10-11). Figure 3 of Hirai is provided hereinbelow.

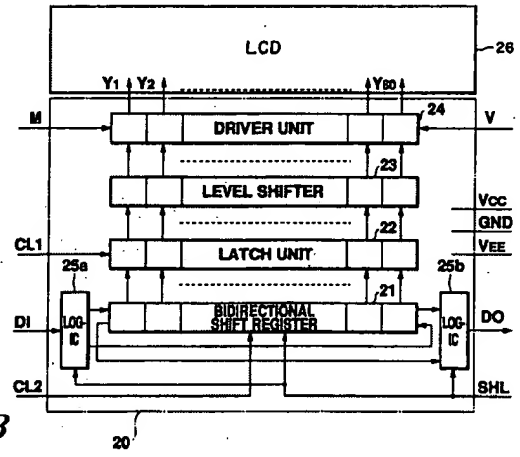


FIG. 3
(PRIOR ART)

Figure 3 of Hirai and Figure 2 of Takeda may reveal, quite possibly, a similarity between element 20 of Hirai and element 13 of Takeda.

In this regard, Figures 4 and 5 of Hirai are provided hereinbelow.

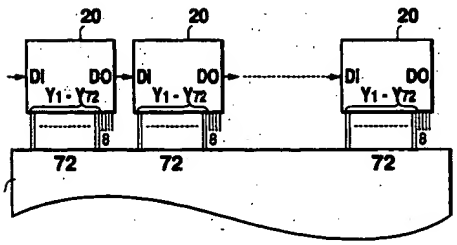


FIG. 4
(PRIOR ART)

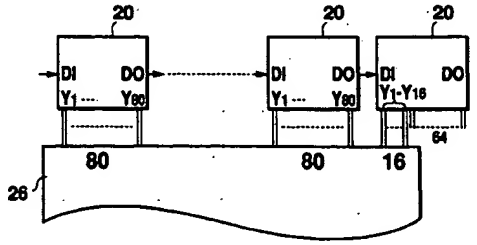


FIG. 5
(PRIOR ART)

Method A requires the circuit configuration as shown in Figure 4, for example (Hirai at column 2, lines 5-6). For method A, because 72 × 8=576, each of ***eight ICs 20*** may be used as a 72-bit output IC without using output pins $Y_{73\text{-}80}$ (eight bits) of each IC 20. (Hirai at column 2, lines 8-10).

Method B requires the circuit configuration as shown in Figure 5, for example (Hirai at column 2, lines 6-7). On the other hand, for method B, because 80 × 7 +16=576, all of ***seven ICs 20*** may be used 80-bit output ICs with the eighth IC 20 as a 16-bit output IC (Hirai at column 2, lines 10-13).

To display a character made up of 16 × 16=256 dots, if method A is used, each of four ICs 20 may be used as a 64-bit output IC; if method B is used, three ICs 20 may be used as 80-bit output ICs with the fourth device of IC 20 as a 16-bit output IC (Hirai at column 2, lines 14-18).

Likewise, to display a character made up of 32 × 32=1024 dots, if method A is used, sixteen ICs 20 may be used as 64-bit output ICs; if method B is used, twelve ICs 20 are used as 80-bit output ICs and eleven ICs 20 are used as 64-bit output ICs (Hirai at column 2, lines 18-23).

Further, to display a character made up of 48 × 48=2304 dots, if method A is used, thirty-two ICs 20 are used as 72-bit output ICs; if method B is used, twenty-eight ICs 20 are used as 80-bit output ICs and one IC 20 is used as a 64-bit output IC (Hirai at column 2, lines 24-28).

- ***Nevertheless, Hirai fails to disclose, teach, or suggest a plurality of driver circuits, said plurality of driver circuits including at least one general driver circuit and one remainder driver circuit.***

- ***Moreover, Hirai fails to disclose, teach, or suggest the quantity of said driver circuit output terminals being the same quantity for said each of said plurality of driver circuits.***

- ***Finally, Hirai fails to disclose, teach, or suggest the quantity of said driver circuits being defined as N/n, wherein "N" is the quantity of said signal lines and "n" is said quantity of said driver circuit output terminals.***

Hayashi - Hayashi arguably teaches that in Figure 1, for example, switching elements $M_{11}, M_{12}, \ldots M_{nm}$ are provided with their directions reversed at every other one and respective picture element electrodes $P_{11}, P_{12}, \ldots P_{nm}$ are each located with a displacement of 1/2 picture element pitch amount (Hayashi at column 3, lines 35-39).

Figure 1 of Hayashi is provided hereinbelow.

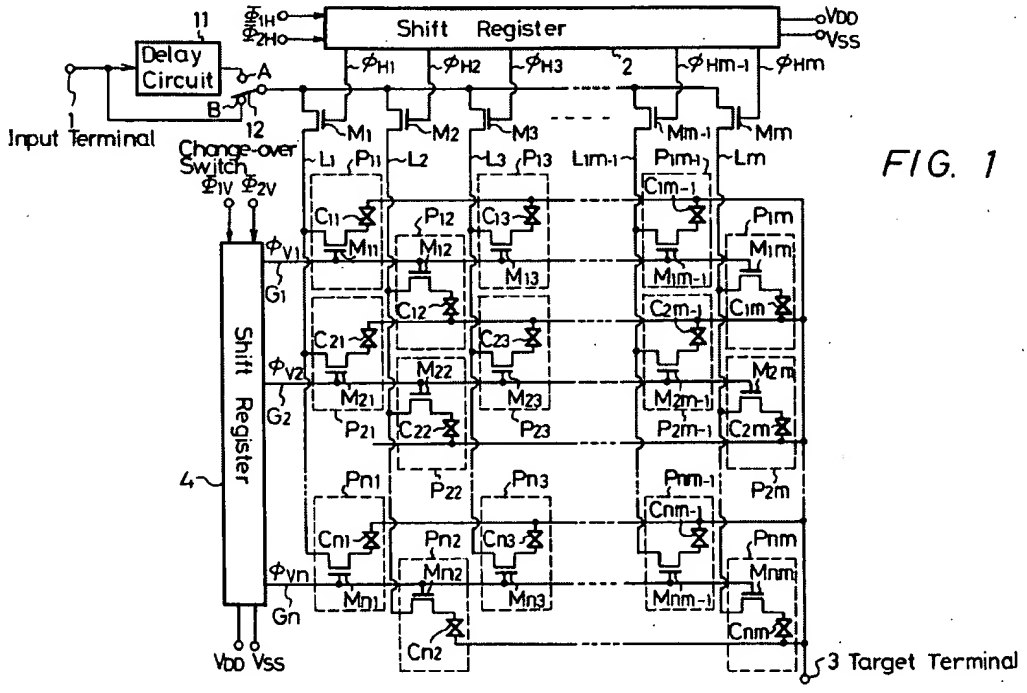


FIG. 1

- ***However, Hayashi fails to disclose, teach, or suggest a plurality of driver circuits, said plurality of driver circuits including at least one general driver circuit and one remainder driver circuit.***

- ***Moreover, Hayashi fails to disclose, teach, or suggest the quantity of said driver circuit output terminals being the same quantity for said each of said plurality of driver circuits.***

- ***Finally, Hayashi fails to disclose, teach, or suggest the quantity of said driver circuits being defined as N/n, wherein "N" is the quantity of said signal lines and "n" is said quantity of said driver circuit output terminals.***

Conclusion

The claims are considered allowable for the same reasons discussed above, as well as for the additional features they recite.

Reversal of the Examiner's decision is respectfully requested.

Dated: September 3, 2008

Respectfully submitted,

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CLAIMS APPENDIX

1-24. (Canceled).

25. A liquid crystal display comprising:

a display portion, said display portion having a plurality of gate lines, a plurality of signal lines and a plurality of pixels,

a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and

a plurality of driver circuits, said plurality of driver circuits including at least one general driver circuit and one remainder driver circuit,

each said at least one general driver circuit having a general driver horizontal shift register circuit and a plurality of general driver circuit output terminals, a general driver circuit output terminal of said plurality of general driver circuit output terminals providing a signal potential to one of said plurality of signal lines,

said remainder driver circuit having a remainder driver horizontal shift register circuit and a plurality of remainder driver circuit output terminals, a remainder driver circuit output terminal of said plurality of remainder driver circuit output terminals providing another signal potential to another of said plurality of signal lines,

the quantity of said remainder driver circuit output terminals being defined as (S – (OP * (DC-1))), "S" being the quantity of said plurality of signal lines, "OP" being the quantity of said general driver circuit output terminals, and "DC" being the quantity of said plurality of driver circuits, and

said quantity of said general driver circuit output terminals being different than said quantity of said remainder driver circuit output terminals.

26. A display according to claim 25, wherein one driver circuit of said plurality of driver circuits is separate and distinct from another driver circuit of said plurality of driver circuits.

27. A display according to claim 25, wherein said plurality of pixels is arranged in a two-dimensional matrix shape.

28. A display according to claim 25, wherein said pixel of said plurality of pixels includes a transistor, a gate electrode of said transistor being electrically connected to said gate line, a source/drain of said transistor being electrically connected to said signal line.

29. A display according to claim 25, wherein said plurality of gate lines is a plurality of rows and said plurality of signal lines is a plurality of columns.

30. (Canceled).

31. A display according to claim 25, wherein a surplus connecting region that does not contribute to said display portion does not occur on the said display.

32-36. (Canceled).

37. A display according to claim 25, wherein an output terminal of said plurality of driver circuits is electrically connected to an input terminal of a time-divisional switch, said time-divisional switch providing a de-multiplexed signal potential to said signal line, said de-multiplexed signal potential being a signal potential for one of a plurality of primary colors that is time-divided from another signal potential for another of said plurality of primary colors and supplied to said signal line.

38-42. (Canceled).

43. A display according to claim 37, wherein said plurality of primary colors is a first primary color, a second primary color and a third primary color.

44. A display according to claim 25, wherein said quantity of general driver circuit output terminals is greater than said quantity of remainder driver circuit output terminals.

45. A display according to claim 25, wherein the sum total of general driver circuit output terminals and said remainder driver circuit output terminals is equal to said plurality of signal lines.

46. A display according to claim 25, wherein said plurality of driver circuits includes more than one said general driver circuit.

47. A display according to claim 46, wherein said each said at least one general driver circuit has an equal number of general driver circuit output terminals.

48. A display according to claim 25, wherein said plurality of driver circuits are driver integrated circuits arranged in an outside of a transparent insulating substrate on which said display portion is formed.

49. A liquid crystal display comprising:

a display portion, said display portion having a plurality of gate lines, a plurality of signal lines and a plurality of pixels,

a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and

a plurality of driver circuits, each of said plurality of driver circuits having a plurality of driver circuit output terminals,

a driver circuit output terminal of said a plurality of driver circuit output terminals providing a signal potential to a signal line of said plurality of signal lines,

the quantity of said driver circuit output terminals being the same quantity for said each of said plurality of driver circuits, and

the quantity of said driver circuits being defined as N/n, wherein "N" is the quantity of said signal lines and "n" is said quantity of said driver circuit output terminals.

50. A display according to claim 49, further comprising:

a plurality of time-divisional switches, said plurality of time-divisional switches receiving said signal potential from said driver circuit output terminal and time-divisionally sending said received signal potential said signal line.

51. A display according to claim 50, wherein the quantity of said time-divisional switches is equal to 3.

52. A display according to claim 49, wherein said quantity of said signal lines is different than said quantity of said driver circuit output terminals.

53. A display according to claim 49, wherein said quantity of said driver circuit output terminals is set to a power of 2.

54. A display according to claim 49, wherein said plurality of driver circuits are driver ICs arranged in an outside of a transparent insulating substrate on which said display portion is formed.

55. A display according to claim 49, further comprising:

a memory circuit for temporarily storing data to be written into said plurality of driver circuits; and

a control circuit for controlling said plurality of driver circuits so as to simultaneously write different data from said memory circuit.

56. A display according to claim 49, wherein a leading waveform and a trailing waveform of a signal output waveform of each of said plurality of driver circuits are symmetrical with respect to a time base.

57. A display according to claim 49, wherein a period of time which is selected by said time-divisional switches is equal to or shorter than 1/3 of a horizontal scanning period.

58. A display according to claim 57, wherein a leading time and a trailing time of each of said plurality of driver circuits are equal to or shorter than the period of time which is selected by said time-divisional switches.

59. A display according to claim 49, wherein a blanking period which is caused for the period of time, selected by said time-divisional switches is equal to or shorter than (a horizontal scanning period - the period of time selected by the time-divisional switches x 3) / 3.

60. A display according to claim 59, wherein said plurality of driver circuits have a function to stop the operation of an output circuit of said plurality of driver circuits for said blanking period.

61. A display according to claim 49, wherein said plurality of driver circuits generate a signal potential so as to correct curves of voltage-transmittance characteristics of R (red), G (green), and G (blue) by diving to said time-divisional switches.

62. A display according to claim 49, wherein within a 1H (H denotes a horizontal scanning period) inversion driving or a 1H common inversion driving, the signal line which is selected first by said time-divisional switches is a line of blue, the signal line which is selected at the second time is a line of green, and the signal line which is selected at the third time is a line of red.

63. A display according to claim 49, wherein within a dot inversion driving, the signal line which is selected first by said time-divisional switches is a line of red, the signal line which is selected at the second time is a line of green, and the signal line which is selected at the third time is a line of blue.

64. A display according to claim 49, wherein time-division of said time-division switches distribute signals to R (red), G (green), and G (blue) constituting one pixel.

65. A display according to claim 49, wherein a surplus connecting region that does not contribute to said display portion does not occur on the said display.

66. A display according to claim 49, wherein said driver circuits is separate and distinct from another driver circuit of said plurality of driver circuits.

67. A display according to claim 49, wherein said each of said plurality of driver circuits has a horizontal shift register circuit.

68. A display according to claim 67, wherein one general driver horizontal shift register circuit of said plurality of driver circuits is separate and distinct from another general driver horizontal shift register circuit of said plurality of driver circuits.

69. A display according to claim 67, wherein said horizontal shift register circuit performs a horizontal scan by sequentially generating horizontal scanning pulses.

70. A display according to claim 67, wherein said horizontal shift register circuit has sampling switches, a level shifter, a data latch circuit, and a digital/analog converting circuit.

71. A display according to claim 25, wherein one general driver horizontal shift register circuit of said plurality of driver circuits is separate and distinct from another general driver horizontal shift register circuit of said plurality of driver circuits.

72. A display according to claim 25, wherein said general driver horizontal shift register circuit performs a horizontal scan by sequentially generating horizontal scanning pulses.

73. A display according to claim 25, wherein said each said at least one general driver circuit has general driver sampling switches, a general driver level shifter, a general driver data latch circuit, and a general driver digital/analog converting circuit.

74. A display according to claim 73, wherein sampling switches in said general driver sampling switches sequentially sample input digital image data in response to horizontal scanning pulses from said general driver horizontal shift register circuit.

75. A display according to claim 73, wherein said general driver level shifter boosts digital data sampled by said general driver sampling switches to digital data of a liquid crystal driving voltage.

76. A display according to claim 73, wherein said general driver data latch circuit is a memory to accumulate digital data boosted by said general driver level shifter by an amount of one horizontal period.

77. A display according to claim 73, wherein said general driver digital/analog converting circuit converts digital data of one horizontal period which is outputted from said general driver data latch circuit into an analog signal and outputs said analog signal.

78. A display according to claim 73, wherein said remainder driver circuit has remainder driver sampling switches, a remainder driver level shifter, a remainder driver data latch circuit, and a remainder driver digital/analog converting circuit.

EVIDENCE APPENDIX

There is no other evidence which will directly affect or have a bearing on the Board's decision in this appeal.

RELATED PROCEEDINGS APPENDIX

There are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.